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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,499	04/12/2004	Kevin P. Grundy	SIPI.P118	3272

7590 01/25/2005

Shemwell Gregory & Courtney LLP
Suite 201
4880 Stevens Creek Boulevard
San Jose, CA 95129

EXAMINER	
BATAILLE, PIERRE MICHE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,499	GRUNDY ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's filed application dated April 12, 2004 with an effective filing dated April 10, 2003. August 14, 2004 responding to advisory action. Applicant's claimed invention has been examined and considered with the results that follow.

Claims 1-27 are pending in the application under examination.

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-27 are rejected under 35 U.S.C. 102(a) as being anticipated by US 2002/0083255 (Greff et al).

With respect to claims 1, Greff discloses a memory system ***(Fig. 1)*** comprising: a memory controller ***(memory controller 31)***; an interface device ***(Interface circuit 30)*** coupled to the memory controller ***(31)*** via a first signal path ***(data bus 28)***; and a

plurality of memory elements ***(DRAM chips provided on modules 24, 26)*** removably coupled to the interface device ***(interface circuit 30)*** via respective second signal paths ***(data bus 32) [second data bus is connected to individual memory devices, DRAM chips, provided on the memory modules 24, 26; paragraph 0031]***, each of the second signal paths having a lower data transfer capacity than a data transfer capacity of the first signal path ***[bus 28 operating at higher transfer speed than bus 32, enabling memory modules 24, 26 to use lower speed memory devices; paragraph 0034; 0040]***.

With respect to claim 17, Greff discloses a method of operation within a memory system, the method comprising: transmitting multiplexed data from a memory controller to an interface device at a first data rate ***[paragraph 0040; 0053]***; demultiplexing the multiplexed data into a plurality of data subsets within the interface device ***multiplexer/demultiplexer 46 for converting the data rate and number of data paths for appropriately coding/decoding the data between buses) [Paragraph 0040]***; and transmitting the each of the data subsets from the interface device to a respective one of a plurality of memory elements at a second data rate ***[paragraph 0040; 0053]***.

With respect to claim 23, Greff discloses an interface device for use in a memory system, the interface device comprising: a first input/output (I/0) port ***(first set of I/O pins 42)*** to receive multiplexed data from a memory controller at a first signaling rate

[paragraph 0040; 0053]; demultiplexing circuitry to demultiplex the multiplexed data into a plurality of data subsets ***(conversion circuit 45 including a multiplexer/demultiplexer 46 for converting the data rate and number of data paths for appropriately coding/decoding the data between buses) [Paragraph 0040]***; and a plurality of second I/O ports to output the plurality of data subsets to respective memory elements at a second signaling rate ***[second set of I/O pins 44 for outputting the converted data; paragraph 0040; 0053]***.

With respect to claim 2, Greff discloses the memory system wherein the first signal path comprises a plurality of substantially parallel signal lines that extend from a first end at the memory controller to a second end at the interface device ***[data bus 28 may have a bus width of any number of parallel data paths; Paragraph 0034]***.

With respect to claim 3, Greff discloses the memory system wherein each of the plurality of the signal lines is disposed within a flexible material to form a flex cable ***[multidrop bus being a bus terminator resistor permitting switchable termination with enable and disable characteristics; paragraph 0032, 0038]***.

With respect to claim 4, Greff discloses the memory system wherein the first signal path further comprises a plurality of shielding elements disposed adjacent individual signal lines of the plurality of signal lines to shield the individual signal lines from one another ***[multidrop bus terminated by a bus terminator resistor permitting protected data transfer; paragraph 0032]***.

With respect to claim 5, Greff discloses the memory system wherein each of the shielding elements is disposed in coaxial alignment with a respective one of the individual signal lines ***[Paragraph 0034, 0053, 0054]***.

With respect to claim 6, Greff discloses the memory system wherein the plurality of signal lines comprise conductive traces disposed on a printed circuit board ***[paragraph 0056]***.

With respect to claims 7 and 26, Greff discloses the memory system wherein the interface device is implemented in a dedicated integrated circuit device ***[paragraph 0056]***.

With respect to claim 8, Greff discloses the memory system wherein the data transfer capacity of the first signal path is at least as great as a sum of the data transfer capacities of the second signal paths ***[Paragraph 0034, 0053, 0054]***.

With respect to claim 9, Greff discloses the memory system wherein the first signal path comprises at least one signal line to conduct a first timing signal from the memory controller to the interface device, and wherein the interface device includes circuitry to sample signals on the first signal path in synchronism with the first timing signal ***[Paragraph 0053; 0054]***.

With respect to claim 10, Greff discloses the memory system wherein the first timing signal is a clock signal ***[paragraph 0034]***.

With respect to claim 11, Greff discloses the memory system wherein the first timing signal is a strobe signal ***[Paragraph 0059]***.

With respect to claim 12, Greff discloses the memory system wherein the second signal paths comprise respective signal lines to conduct second timing signals from the interface device to the memory elements, and wherein the first timing signal oscillates at greater frequency than the second timing signals ***[Paragraph 0059, 0034]***.

With respect to claim 13, Greff discloses the memory system wherein the oscillating frequency of the first timing signal is an integer multiple of the oscillating frequency of the second timing signals ***[Paragraph 0059, 0034]***.

With respect to claim 14, Greff discloses the memory system wherein at least one of the memory elements comprises a memory module having a plurality of discrete memory devices mounted thereon ***[paragraph 0055]***.

With respect to claim 15, Greff discloses the memory system wherein at least one of the memory elements comprises a plurality of memory modules coupled in parallel to the respective second signal path ***[paragraph 0055]***.

With respect to claim 16, Greff discloses the memory system wherein at least one of the memory elements comprises a discrete semiconductor memory device ***[paragraph 0055]***.

With respect to claims 18 and 24, Greff discloses the method wherein the second data rate is lower than the first data rate ***[Paragraph 0034, 0059]***.

With respect to claims 19 and 25, Greff discloses the method wherein the first data rate is an integer multiple of the second data rate ***[Paragraph 0034, 0059]***.

With respect to claim 20, Greff discloses the method further comprising receiving the multiplexed data within the memory controller ***[Paragraph 0047]***.

With respect to claim 21, Greff discloses the method further comprising receiving a plurality of data values from a host device, and wherein transmitting multiplexed data from the memory controller to the interface device comprises transmitting the plurality of data values to the interface device in respective time intervals ***[Paragraph 0034, 0053, 0054]***.

With respect to claims 22 and 27, Greff discloses the method wherein demultiplexing the multiplexed data into a plurality of data subsets comprises allocating multiplexed data received in the interface device during a first time interval to a first one of the data subsets and allocating multiplexed data received during a second time interval to a second one of the data subsets ***[Paragraph 0034, 0053, 0054]***.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 2002.0067915 (Shida et al) teaching interface system for receiving data packet from digital transmission line.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (9:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

January 21, 2005

PIERRE BATAILLE
PRIMARY EXAMINER